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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,135	09/10/2003	Dureseti Chidambarao	FIS920030184US1	2134
29625	7590	08/11/2004	EXAMINER	
MCGUIRE WOODS LLP 1750 TYSONS BLVD. SUITE 1800 MCLEAN, VA 22102-4215			KILDAY, LISA A	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/605,135	Applicant(s) CHIDAMBARRAO ET AL.	
	Examiner Lisa Kilday	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on election on 6/28/4.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-13 and 20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 20 is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-8, 12 and 13 is/are rejected.
- 7) ☒ Claim(s) 5 and 9-11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 9/3 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>11/3</u> . | 6) <input type="checkbox"/> Other: _____  |

### ***Drawings***

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "32". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

Claim 1 is objected to because of the following informalities: claim 1, line 8 recites the limitation of "the polysilicon from a gate of the p-type transistor." For form and clarity, the preamble of claim 1 should be amended to state: an n-type transistor and a p-type transistor --having a polysilicon gate-- because it is understood that a transistor has a polysilicon gate. Appropriate correction is required.

Claim 5 is objected to because of the following informalities: in line 2, replace "HF" with --Hf--.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6-8,12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic et al. (6,512,273) in view of Kim et al. (5,677,232).

In re claim 1, Krivokapic et al. in fig. 2a-d teaches a method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor (14) and a p-type transistor (16), the method comprising: depositing oxide (18) on the n-type transistor (14) and the p-type transistor (16) the n-type transistor (14) and the p-type transistor (16) each having spacers (ref. 20, 33; step 50 in fig. 1; col. 4, lines 53-57) are surrounded with oxide (18; step 64 in fig. 1), etching a portion of the polysilicon from a gate of the p-type transistor (step 80 in fig 1; col. 5, lines 19-22); depositing a low-resistance material on the p-type transistor and the n-type transistor (step 80 deposits polysilicon and step 50 deposits Silicon nitride; col. 4, lines 53-56; col. 5, lines 19-22); and heating the integrated circuit such that the deposited low-resistance material reacts with the polysilicon of the p-type transistor and the polysilicon of the n-type transistor (step 90 in fig. 1; col. 5, lines 30-32). Kim et al. teaches that the compressive mechanical stresses of the polysilicon of the p-type transistor and the polysilicon of the n-type transistor that are formed along a

longitudinal direction of a channel of the p-type transistor and this property is an *inherent property* of the polysilicon of the p-type transistor and the polysilicon of the n-type transistor (see Kim et al. col. 4, lines 52-60). Krivokapic et al. teaches forming the polysilicon of the p-type transistor and the polysilicon of the n-type transistor, which inherently contain the characteristic of compressive mechanical stresses that are formed along a longitudinal direction of a channel of the p-type transistor.

Krivokapic et al. teaches depositing oxide (18) on the n-type and p-type transistors (step 48; col. 4, lines 52-53). However, Krivokapic et al. does not teach chemical/mechanical polishing ("CMP") the deposited oxide such that a gate stack of the n-type transistor and a gate stack of the p-type transistor. However, Kim et al. teaches in figure 10, depositing oxide (31) over the gate stack of the transistors and etching back the deposited oxide with CMP (col. 5, lines 5-7). Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify the process of Krivokapic et al. by chemically mechanically polishing the deposited oxide in order to expose the gate stack of the transistors.

In re claim 2, Krivokapic et al. teaches removing a portion of the deposited low resistance material (for Silicon nitride- step 50; for polysilicon step 80).

In re claim 3, Krivokapic et al. teaches covering n-type transistor with a mask (step 52) prior to etching; and removing the mask after performing the etching (step 56; col. 4, lines 53-61).

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In re claim 4, Krivokapic et al. teaches wherein the mask is a patterned photoresist layer (12).

In re claim 6, Krivokapic et al. teaches removing a portion of the deposited low-resistance material with a selective etching technique (col. 4, lines 53-56; col. 5, lines 19-22).

In re claim 7, Krivokapic et al. teaches wherein the step of heating comprises heating the integrated circuit to a temperature of about 300 to about 1000°C (col. 5, lines 30-31).

In re claim 8, Krivokapic et al. teaches wherein the step of depositing a low-resistance material comprises depositing a low-resistance material to a height of approximately 30-200 Å (col. 5, lines 19-21). Krivokapic et al. teaches depositing the low-resistance material to 250 Å, followed by etching the low-resistance material. Therefore, it would have been obvious to one skilled in the art that Krivokapic et al. deposits the low-resistance material at 250 Å, then etches the material down to a thickness of approximately 200 Å in order to form spacers.

In re claim 12, Krivokapic et al. teaches wet etching of the polysilicon (col. 5, line 6).

In re claim 13, Krivokapic et al. teaches depositing a low-resistance material on the p-type and n-type transistor (step 80 deposits polysilicon and step 50 deposits Silicon nitride; col. 4, lines 53-56; col. 5, lines 19-22). However, Krivokapic et al. is silent on the method of deposition. However, Kim et al. teaches depositing the low-resistance material by CVD (col. 5, lines 3-5).

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Therefore it would have been obvious to one skilled in the art to modify the process of Krivokapic et al. by depositing the low-resistance material by CVD for the purpose of precisely forming the layer of low-resistance material.

***Allowable Subject Matter***

Claim 20 allowed.

The following is an examiner's statement of reasons for allowance:

Krivokapic et al. teaches a method for manufacturing an integrated circuit including an n-type and p-type transistor, the method comprising: forming a polysilicon layer on the n-type and p-type transistor, depositing a low-resistance material on the p-type and n-type transistor; and heating the integrated circuit such that the deposited low-resistance material reacts with the polysilicon (col. 4, line 40 – col. 5, line 36). The inherent property of forming compressive mechanical stresses along a longitudinal direction of a channel of the p-type transistor is taught in Kim et al. Prior art does not teach or suggest the limitations above *in combination with* forming the polysilicon layer on the p-type transistor that has a shorter height than the polysilicon layer on the n-type transistor in order to reduce the compressive stresses along a longitudinal direction of the p-type transistor by selective etching the polysilicon layer over both the p-type and n-type transistors.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claims 5, 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: in re claim 5, prior art does not teach or suggest depositing Co, Hf, Mo, Ni, Pd<sub>2</sub>, Pt, Ta, Ti, W, and Zr on the p-type and n-type transistor in order to form a self-aligned silicide.

In re claim 9, prior art does not teach or suggest wherein the etching the polysilicon comprises etching about half of the polysilicon of the p-type transistor where the polysilicon layer on the p-type transistor has a shorter height than the polysilicon layer on the n-type transistor in order to reduce the compressive stresses along a longitudinal direction of the p-type transistor by selective etching the polysilicon layer over both the p-type and n-type transistors.

In re claim 10, prior art does not teach or suggest etching the polysilicon from the gate of the p-type transistor such that the ratio of n-type polysilicon to p-type polysilicon is about 2:1 in order to reduce the compressive stresses along a longitudinal direction of the p-type transistor by selective etching the polysilicon layer over both the p-type and n-type transistors.

In re claim 11, Krivokapic et al. teaches etching the p-type polysilicon (col. 5, lines 19-22). Prior art does not teach or suggest etching the p-type polysilicon to about 250-750 Å, which would further reduce the compressive stresses along a longitudinal direction of the p-type transistor by selective etching.

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**Conclusion**

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0957. See MPEP 203.08.

Any inquiry concerning this communication from the examiner should be directed to Lisa Kilday whose telephone number is (571) 272-1962. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo, can be reached on (571) 272-1957. The fax number for the group is (703) 872-9306. MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

Lisa Kilday

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8/9/04

*LISA K. LIDAY*  
*Patent Examiner*  
*AU 2829*